What is claimed is:

1. A reconfigurable emulation integrated circuit, comprising:

a storage unit comprising a signal inclusion schedule; and

circuitry, coupled to the storage unit, operative to generate and transmit a message outside the emulation integrated circuit, the message comprising a plurality of signals and assembled in accordance with the signal inclusion schedule, wherein the signal inclusion schedule specifies the order and frequency of occurrence of each of the plurality of signals in the message.

2. The message formation and send block of claim 1, wherein signals in the message that are determined to be more critical than other signals occur with greater frequency than signals determined to be less critical in the signal inclusion schedule.

3. The message formation and send block of claim 1, wherein the message is generated and transmitted in a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

4. The message formation and send block of claim 1, wherein the circuitry further includes a parity value generator and wherein the message further comprises a parity value generated by the parity value generator.

5. A method in a reconfigurable logic chip, comprising steps of:

determining a criticalness of each of a plurality of signals to be sent over a single output of the reconfigurable logic chip;

preparing a signal inclusion schedule based on the criticalness of each of the plurality of signals, wherein signals of greater criticalness occur with greater frequency than signals of lesser criticalness; and

sending the plurality of signals over the single output based on the signal inclusion schedule.

6. The method of claim 5, wherein sending the plurality of signals over the single output comprises steps of:

generating a message comprising state values of the plurality of signals; and

transmitting the message over the single output.

7. The method of claim 6 wherein generating and transmitting the message are performed over a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

8. The method of claim 5, further comprising steps of:

generating a parity value based on the plurality of signals; and

sending the generated parity value over the single output.

9. A reconfigurable integrated circuit, comprising:

a storage unit comprising a signal inclusion schedule for a plurality of signals to be received in a message; and

circuitry, coupled to the storage unit, operative to receive and extract the plurality of signals from the message in accordance with the signal inclusion schedule, wherein the signal inclusion schedule specifies the order and frequency of occurrence of each of the plurality of signals in the message.

10. The message receive and disassembly block of claim 9, wherein signals in the message that are determined to be more critical than other signals occur with greater frequency than signals determined to be less critical in the signal inclusion schedule.

11. The message receive and disassembly block of claim 9, wherein the message comprises state values of the plurality of signals.

12. The message receive and disassembly block of claim 9, wherein the message is received and disassembled in a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

13. The message receive and disassembly block of claim 9, wherein a parity value is extracted from the message.

14. The message receive and disassembly block of claim 13, wherein the circuitry further a portion configured to generate a parity verification value from the extracted plurality of signals and compare the parity verification value with the extracted parity value.

15. A method, comprising steps of:

determining a criticalness of each of a plurality of signals;

preparing an inclusion schedule based on the criticalness of each of the plurality of signals, wherein signals of greater criticalness occur with greater frequency than signals of lesser criticalness; and

receiving the plurality of signals over a single input based on the inclusion schedule.

16. The method of claim 15, wherein receiving the plurality of signals over the single input comprises steps of:

receiving a message comprising state values of the plurality of signals over the single input; and

extracting the state values of the plurality of signals that form the message.

17. The method of claim 16, wherein the steps of receiving and extracting are performed over a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

18. The method of claim 15, further comprising steps of:

receiving a parity value;

generating a parity verification value from the received plurality of signals; and

comparing the received parity value with the generated parity verification value.

19. A method of transferring multiple signals over a single interconnect, comprising steps of:

determining a priority level of each of the multiple signals;

generating a signal transfer schedule defining some of the multiple signals to be transmitted more often than others of the multiple signals;

transmitting the multiple signals over the single interconnect in accordance with the signal transfer schedule; and

receiving the multiple signals over the interconnect in accordance with the signal transfer schedule.

20. An emulation integrated circuit, comprising:

at least one reconfigurable logic resource;

at least one output pin; and

a message formation and send block in communication with the output pin and the reconfigurable logic resource, the message formation and send block operative to receive multiple output signals from the reconfigurable logic resource and generate a message on the output pin in accordance with a first signal inclusion schedule, wherein the first signal inclusion schedule specifies the order and frequency of occurrence of each of the output signals.

21. The emulation integrated circuit of claim 20, further comprising:

an input pin; and

a message receive and disassembly block in communication with the input pin and the reconfigurable logic resource, operative to receive a message and extract multiple input signals from the message in accordance with a second signal inclusion schedule.

22. The emulation integrated circuit of claim 20, further comprising a plurality of output pins and a plurality of message formation and send blocks in communication with the plurality of

output pins and the reconfigurable logic resource, each message formation and send block operative to receive multiple output signals from the reconfigurable logic resource and generate a message on the output pin in accordance with a different respective signal inclusion schedule.

23. The emulation integrated circuit of claim 20, further comprising a plurality of reconfigurable logic resources in communication with the message formation and send block.

24. An emulation integrated circuit, comprising:

at least one reconfigurable logic resource;

at least one input pin; and

a message receive and disassembly block in communication with the reconfigurable logic resource and the input pin, the message receive and disassembly block operative to receive a message by the input pin and extract multiple input signals for the reconfigurable logic resource in accordance with a signal inclusion schedule, wherein the signal inclusion schedule specifies the order and frequency of occurrence of each of the input signals.

25. An interconnect integrated circuit, comprising:

at least one reconfigurable routing matrix;

at least one output pin; and

a message formation and send block in communication with the output pin and the routing matrix, the message formation and send block operative to receive multiple output signals from the reconfigurable logic resource and to generate a message containing the output signals on the output pin in accordance with a first signal inclusion schedule, wherein the first signal inclusion schedule specifies the order and frequency of occurrence of each of the output signals.

26. The interconnect integrated circuit of claim 25, further comprising:

an input pin; and

a message receive and disassembly block in communication with the input pin and routing matrix, the message receive and disassembly block operative to receive a message and extract multiple signals from the message in accordance with a second signal inclusion schedule.

27. An interconnect integrated circuit, comprising:

at least one routing matrix;

at least one input pin; and

a message receive and disassembly block in communication with the routing matrix and the input pin, the message receive and disassembly block operative to receive a message via the input pin and extract multiple input signals for the routing matrix in accordance with a signal inclusion schedule, wherein the signal inclusion schedule specifies the order and frequency of occurrence of each of the input signals.